CS 210 Final Exam Solutions

Alex Vondrak

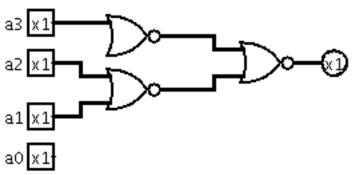
Spring 2012

1. Let the BCD digit $d = a_3a_2a_1a_0$. Then, the circuit has the following outputs.

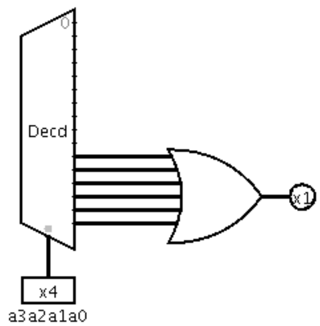
a_3a_2 \ a_1a_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

Minimum-literal product of sums: $(a_3' + a_2'a_1')' = a_3(a_2 + a_1)$
Sum of minterms: $\sum(10, 11, 12, 13, 14, 15)$

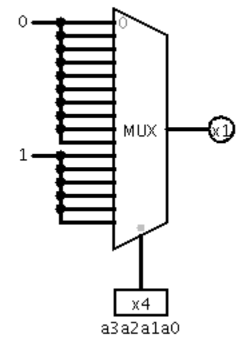
(a)



(b)



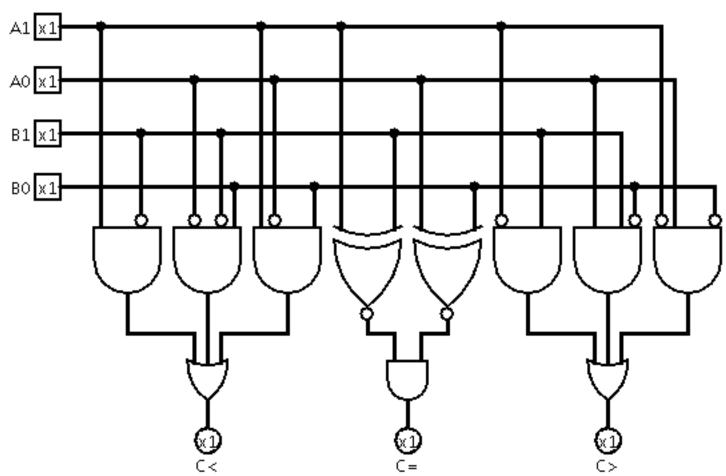
(c)



2.

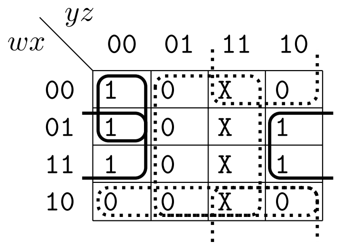
A_1A_0 \ B_1B_0	00	01	11	10
00	=	<	>	>
01	>	=	>	>
11	<	<	=	>
10	<	<	<	=

$$C_< = A_1B_1' + A_0'B_1'B_0 + A_1A_0'B_0$$
$$C_= = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$$
$$= (A_1 \oplus B_1)'(A_0 \oplus B_0)'$$
$$C_> = A_1'B_1 + A_0B_1B_0' + A_1'A_0B_0'$$



3.

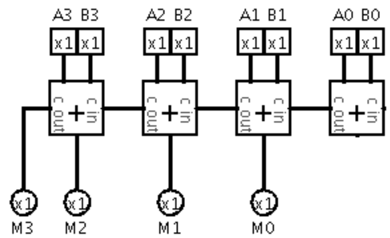
(a)



(b)

- Minimum sum of products: $e = xz' + w'y'z'$
- Minimum inverted sum of products: $e' = z + wx' + x'y$
  $\implies e = (z + wx' + x'y)'$
- Minimum product of sums: $e = (z + wx' + x'y)' = z'(w' + x)(x + y')$
- Minimum inverted product of sums: $e = xz' + w'y'z' = ((x' + z)(w + y + z))'$

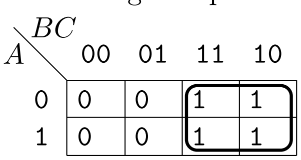
4.



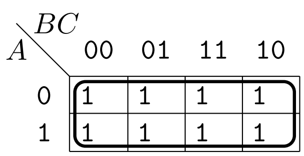
5. **1, 2, 3, 4.** State Table:

Present State			Circuit Input	Circuit Output	Next State			Flip-Flop Inputs		
A	B	C	*–none–*	*–none–*	A	B	C	TA	TB	TC
0	0	0			0	1	0	0	1	0
0	0	1			0	1	1	0	1	0
0	1	0			1	0	0	1	1	0
0	1	1			1	0	1	1	1	0
1	0	0			1	1	0	0	1	0
1	0	1			1	1	1	0	1	0
1	1	0			0	0	0	1	1	0
1	1	1			0	0	1	1	1	0

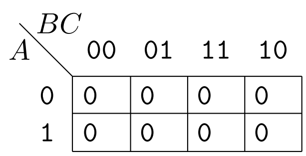
5. Karnaugh Maps:



TA = B

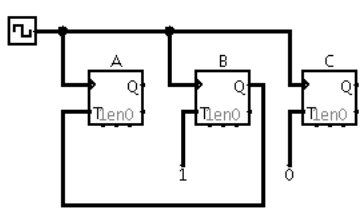


TB = 1



TC = 0

6. Logic Diagram:



6. **1.** Circuit Output Expressions:

$$y = (A \oplus B) \oplus x$$

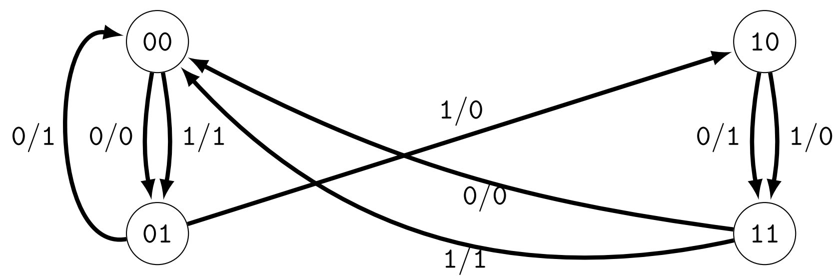
Flip-Flop Input Expressions:

$$\text{JA} = (((A \oplus B)x)'(AB)')'$$
$$\text{KA} = B$$
$$\text{DB} = B'$$

2, 3, 4. State Table:

Present State		Circuit Input	Circuit Output	Next State		Flip-Flop Inputs		
A	B	x	y	A	B	JA	KA	DB
0	0	0	0	0	1	0	0	1
0	0	1	1	0	1	0	0	1
0	1	0	1	0	0	0	1	0
0	1	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	1
1	0	1	0	1	1	1	0	1
1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	1	1	0

State Diagram:



7. (a)

	Register A	Register B	Register P
Initially:	0010	0011	0000
After pulse 1:	0001	0110	$0000 + 0000 = 0000$
After pulse 2:	0000	1100	$0000 + 0110 = 0110$
After pulse 3:	0000	1000	$0110 + 0000 = 0110$

We can see after 2 clock cycles that the contents of P will no longer change on this example, since A has been emptied.

(b) This circuit multiplies the contents of registers A and B (storing the result in register P) using the grade-school multiplication algorithm:

$A =$			1	0	
$B =$			1	1	
			0	0	$\leftarrow 0011 \times 0 = 0000$
		1	1		$\leftarrow 0110 \times 1 = 0110$
$P =$	0	1	1	0	$\leftarrow$ sum of intermediate results