CS 210—Computer Logic
Spring 2012

MWF 9:15 AM–10:20 AM, Room 8-302

Alex Vondrak — Office 8-39
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www.csupomona.edu/~ajvondrak/cs/210 — MWF 12:00 PM–2:00 PM

Text Book

M. Morris Mano and Michael D. Ciletti. *Digital Design. With An Introduction to the Verilog HDL*. 5th ed. Pearson. ISBN: 978-0-13-277420-8.

Craig A. Rich (Spring 2012). *Computer Logic. CS 210 Lecture Notes*. Available at the Bronco Copy 'n Mail in the Bronco Student Center.

Grading

Exams 60%
- Midterm (tentatively Friday April 27) 30%
- Final (Monday June 4, 9:10 AM–11:10 AM) 30%

Homework 40%

The overall course grades will be assigned according to the standard "flat" scale:

A	B	C	D	F
$\geq 90\%$	$\geq 80\%$	$\geq 70\%$	$\geq 60\%$	$\geq 0\%$

However, I reserve the right to curve grades if necessary (with the median student typically earning a `C` or `C+`). Pluses and minuses will be assigned based on how well I feel you've done within your grade bracket.

As a rule, late homework will not be accepted.

Homework will involve constructing simulated circuits using the Java application *Logisim*, available at `http://ozark.hendrix.edu/~burch/logisim/`.

You may work with others to figure out how to do the homework, but be sure to work on your own when writing the problems up (in code or otherwise). Rule of thumb: discussing is okay, but do not ask to look at someone else's homework, and do not offer to let others look at yours. If I suspect two assignments are copies of each other, both will receive scores of 0.

There will be no make-ups for exams without prior approval.

Coverage

The course will cover most of the topics in Chapters 1–6 of *Digital Design*.